

# FINAL REPORT

## *MONOLITHIC DIODE ARRAYS FOR QUASIOPTICAL MILLIMETER WAVE BEAM STEERING*

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## 1.0 INTRODUCTION

This final report presents the details of the research and design effort for the first phase of a program to produce a monolithic diode array for quasioptical beam steering at millimeter wavelengths. During Phase 1 we developed the design for Schottky varactor diodes and incorporated this device design into the design of an optical mesh phase shifting array. We have processed  $12.7 \times 12.7 \text{ mm}^2$  dies on GaAs and have completed DC measurements on the diodes in these samples. In this report we present the diode design and dc test results, the drive circuit design, the phase shifting array design, the status of the specially designed RF test set up, and an outline of how the work will be continued into Phase 2.

Electronic beam steering is accomplished by adding a linear phase shift across the aperture of an antenna. The optical principle is based on a simple diffraction model as shown in Fig.1 [Goldsmith, 1989], where  $d = 2\pi/\lambda dx \sin\theta$ . In this Figure  $dx$  can be the spacing between feed elements in a traditional phased array or it can represent the spacing between active elements in a monolithic array. For small angles the total phase shift across an aperture having diameter  $D$  is  $\Delta\phi = 2\pi D\theta/\lambda$ . To scan the antenna beam by an angle  $\theta$  requires a phase shift every distance  $dx$  equal to  $2\pi/\lambda$  times  $\theta$ .

The quasioptical circuit comprises a 2-dimensional square metallic mesh on gallium arsenide loaded with Schottky varactor diodes. The mesh is an inductive element and the diodes have a variable capacitance which is controlled by the bias voltage. The phase of a wave transmitted through the monolithic array is changed by an amount determined by the diode capacitance. To simplify the problem we designed an array which reflects instead of transmits, thereby requiring only 1/2 the amount of phase shift on each pass. Fig.2 shows the schematic of the electronically controllable phase shifting array [1]. This design also simplifies the biasing of the array.

The proposed beam steering array layout is shown in Fig.3. The array has a 115 mm diameter with a square hole in the center for the focal plane antenna elements. The  $12.7 \text{ mm}$  squares show the location of the individual die. Each die is biased separately by a six layer drive circuit described in Section 3.0, thus giving the desired phase shift across the aperture of the antenna. All diodes on a given die are biased the same.

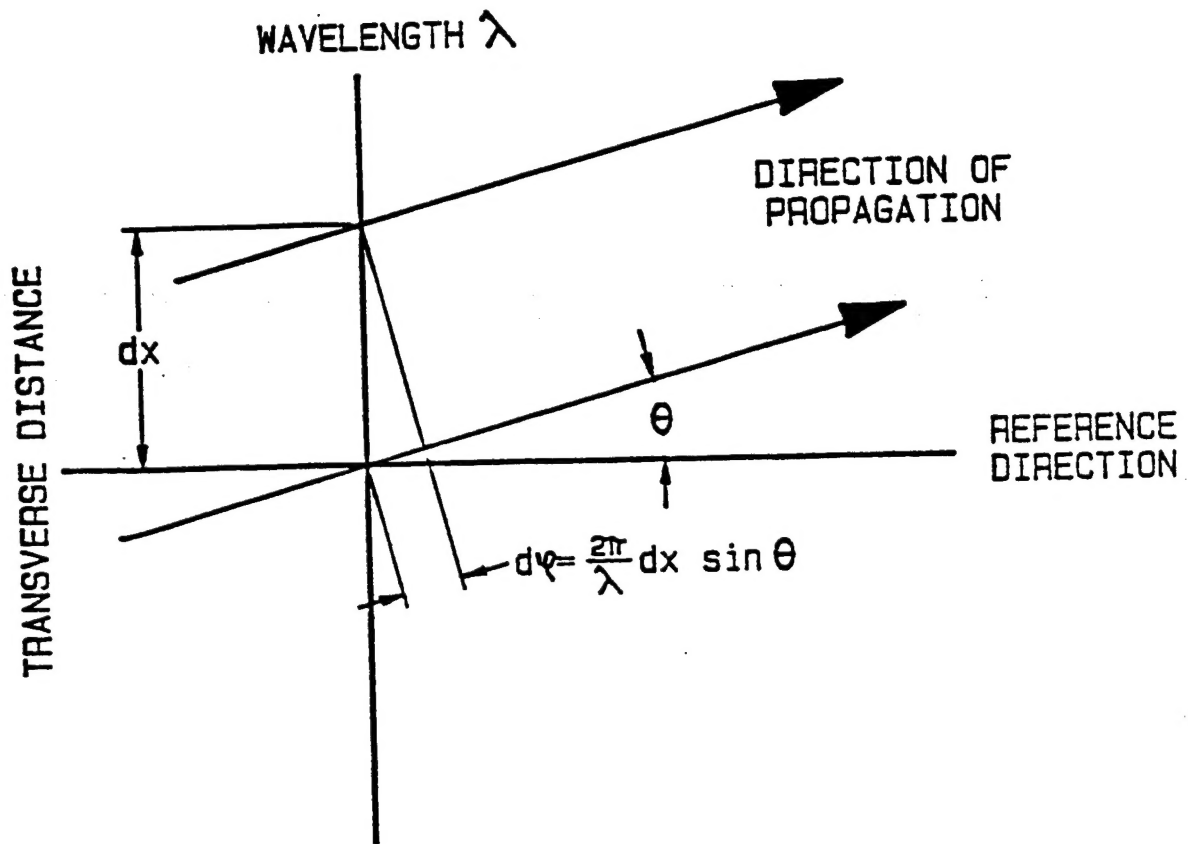


Figure 1 LINEAR PHASE GRADIENT FROM BEAM SCANNING

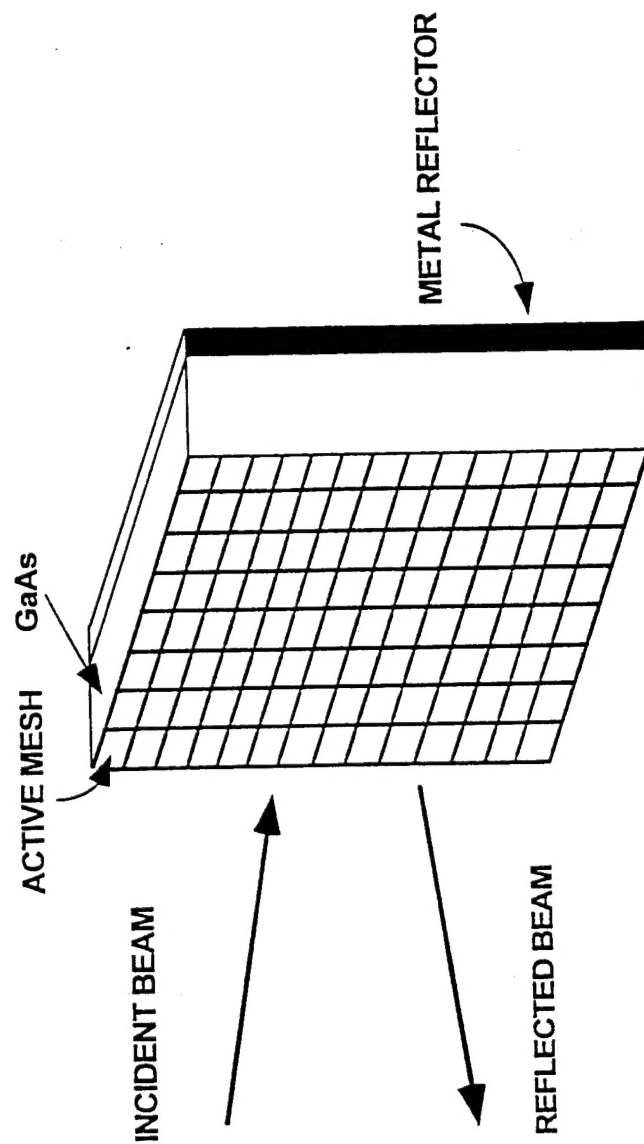
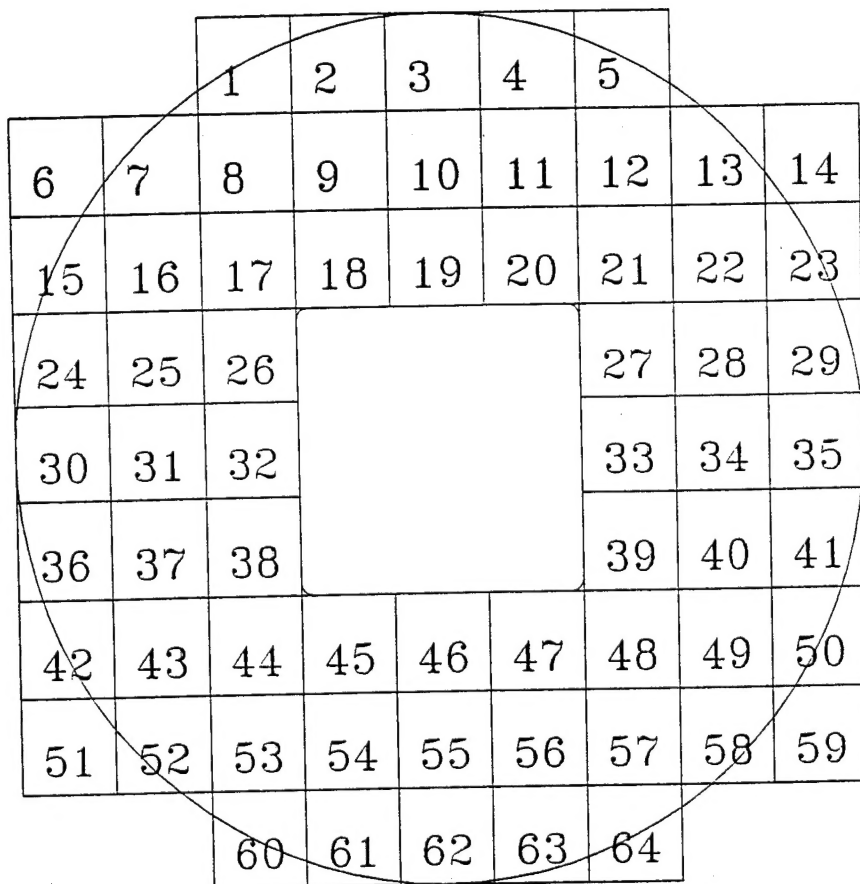


Figure 2 SCHEMATIC OF THE ELECTRONICALLY CONTROLLABLE  
PHASE SHIFTING ARRAY



**Figure 3 BEAM STEERING ARRAY LAYOUT**

Upon completion of Phase 2 our immediate application of this beam steering array will be to achieve super-resolution in a compact imaging camera.

## **2.0 MONOLITHIC VARACTOR DIODE PHASE SHIFTING ARRAY**

The idea of using the diode grids for electronic beam steering was introduced by Lam et al. [1]. As shown in Fig.2, when an incident beam reflects off the diode grid, the direction of the reflected wave can be controlled by progressively varying the reflection phase across the grid. The reflection phase of the diode grid can be controlled by varying the DC bias on the diodes. We plan to develop a monolithic Schottky varactor diode phase shifter on GaAs substrate. For this we have to address two design issues — device design as well as the embedding circuit design.

### **2.0.1. DEVICE DESIGN** **— SCHOTTKY VARACTOR DIODE**

The critical element of our monolithic phase-shifting array is the planar Schottky diode. One aim of this work is to design a Schottky varactor diode which demonstrates maximum possible capacitance variation with bias voltage.

All varactors depend on a nonlinear capacitance-voltage and some type of barrier to real current flow. The most common is the reverse biased Schottky varactor diode. This diode consists of a Schottky contact on top of a doped semiconductor with a back ohmic contact. Fig.4 shows the schematic diagram of a circular anode Schottky varactor diode. The metal-semiconductor junction forms a barrier to electron flow while the semiconductor depletion region forms a capacitor with the well known inverse-square-root voltage dependence.

The three most important circuit parameter of a varactor are the breakdown voltage, zero bias capacitance and the series resistance. They affect the level of impedance the varactor will present, the amount of power the varactor will handle and the amount of power the varactor will dissipate in a circuit. A higher phase range can be achieved for a single grid by increasing the capacitance ratio of the device. Our goal is to design an epitaxial profile that will provide a suitable capacitance-voltage



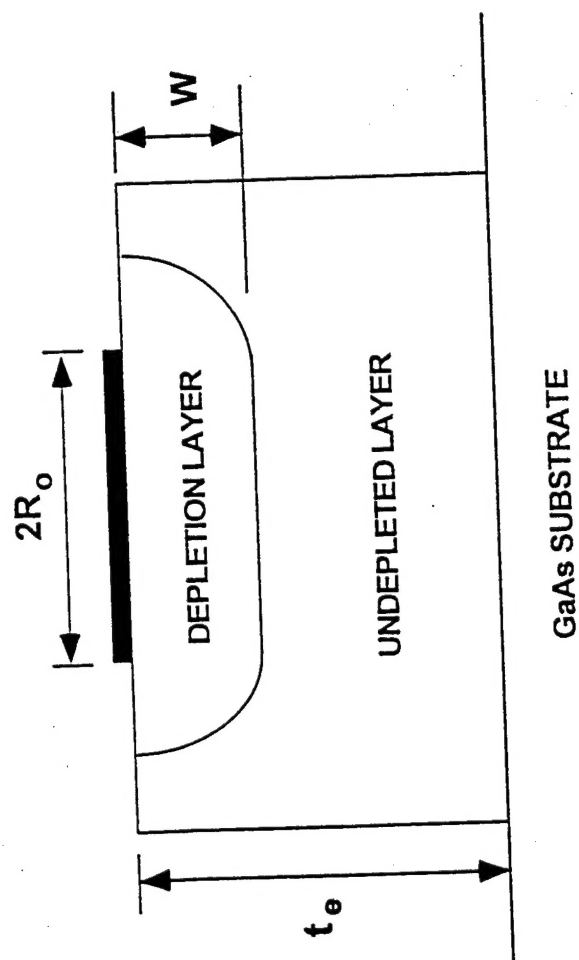


Figure 4 SCHEMATIC DIAGRAM OF A CIRCULAR ANODE SCHOTTKY VARACTOR DIODE

characteristics with a minimum series resistance and higher breakdown voltage.

#### a) DEVICE PHYSICS AND CIRCUIT MODEL

The circuit model of a varactor diode is shown in the Fig.5, where  $C_j$  is the voltage variable capacitance of the depletion region,  $R_j$  is the junction resistance of the depletion region and  $R_s$  is the series resistance of the diode. The modulation of the junction capacitance with bias voltage is used for the phase variation.

The gallium arsenide (GaAs) is chosen rather than other semiconductors because of its high mobility, easy isolation and good Schottky contact. At 94 GHz, the absorption loss for a Cr-doped 20 mils thick GaAs is negligible ( about 0.013 dB, calculated from data in [2] ).

The structure used in this study has a hyperabrupt doping profile, i.e. the net doping concentration of the epitaxy decreases with the distance from the metal-semiconductor interface. For the same voltage variation, the capacitance of a hyperabrupt junction changes more than that of a comparable abrupt junction device. This should result in an improved beam steering array because phase shift depends upon the nonlinearity of the capacitance-voltage law.

The doping concentration is given by

$$N_d(x) = x_0 + N_0 \exp(-x/L) \quad (1)$$

where  $N_0$  is the impurity atom concentration at the surface,  $x_0$  is the zero bias depletion width and  $L$  is the characteristic length of the exponential decay. The design method is based on Lundien et al.'s [3] design algorithm of an exponentially retrograded doping profile. In the depletion approximation, the one dimensional Poisson equation,

$$d^2\phi/dx^2 = -qN_d/\epsilon_s \quad (2)$$

is integrated where  $\phi$  is the electric potential,  $q$  is the electronic charge, and  $\epsilon_s$  is the dielectric permittivity of the semiconductor. The boundary conditions are  $\phi(x=0)=0$  and  $f(x=W_{dep})=\phi_j - V_{app}$ , where  $\phi_j$  is the junction potential,  $W_{dep}$  is the depletion width of the space charge region, and  $V$  is the applied voltage. This leads to an algebraic relation,  $V_{app} = F(W_{dep})$ , which is used to compute the corresponding CV relation

$$C = \epsilon_s A / W_{dep} \quad (3)$$

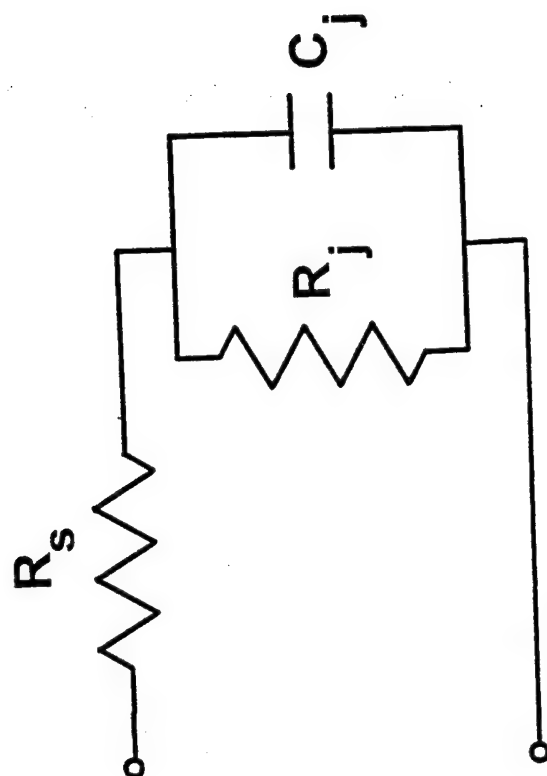


Figure 5 CIRCUIT MODEL OF A VARACTOR DIODE

where A is the area of the varactor.

For the circular anode as shown in Fig.4, the junction capacitance is given by

$$C_j = (\epsilon_s A / W) + (3\epsilon_s A) / (2R_o) \quad (4)$$

where  $R_o$  is the anode radius [4].

The junction resistance,  $R_j$  represents the conduction current through the Schottky barrier, and is a parasitic element for the varactor operation. This effect is minimized by confining the applied voltage values between the point at which forward current becomes significant, i.e., between the device turn-on and the reverse breakdown limit.

The low frequency series resistance of the device is due to the resistance of the undepleted region, the substrate and the ohmic contact.

$$R_s = R_{epi} + R_{sub} + R_{ohm} \quad (5)$$

The largest component of the series resistance is due to the undepleted epitaxial layer, which is calculated from,

$$R_{epi} = \int_{W_{dep}}^{T_{epi}} dx / (q\mu_n N_d A) \quad (6)$$

where  $\mu_n$  is the electron mobility and  $T_{epi}$  is the epitaxial thickness. An empirical expression for the electron mobility is used

$$\mu_n = (10^4) / (1 + \sqrt{N_d / (10^{17})}) \quad (7)$$

where  $N_d$  is in units of  $\text{cm}^{-3}$  and  $\mu_n$  is in units of  $\text{cm}^2(\text{Vs})^{-1}$  [5].

The substrate series resistance is

$$R_{sub} = 1 / (4R_o \sigma_{sub}) \quad (8)$$

where  $\sigma_{sub}$  is the substrate conductivity and  $R_o$  is the anode radius. The substrate is usually highly doped to minimize the substrate resistance. The ohmic contact resistance is given by,

$$R_{oc} = R_{sc} / A_{oc} \quad (9)$$

where  $A_{oc}$  is the ohmic contact area and  $R_{sc}$  is the ohmic contact specific resistance.

The voltage applied to a Schottky diode operating in the varactor mode is generally bounded by the diode turn-on voltage in the forward direction and by voltage breakdown in reverse direction. Neglecting the tunneling, the reverse breakdown is caused by avalanche multiplication [6]. Depending on the device design, reverse breakdown can occur while the depletion edge is still in the active layer, or it can occur after the depletion edge has crossed the active/buffer layer interface, or 'punched-through'. Avalanche breakdown is the result of a multiplicative effect involving the creation of electron-hole pairs. An electron which gains sufficient energy from the electric field across the depletion region can, upon collision with an atom, break a lattice bond and create an electron-hole pair. If the electron-hole pair is sufficiently excited by the electric field, it can in turn create additional electron-hole pairs. The voltage at which this process becomes a chain reaction, is the breakdown voltage. To obtain the maximum capacitance variation and to reduce the diode series resistance, the active layer thickness is chosen so that punch-through occurs at the same time the critical field is reached.

The breakdown voltage is computed as the applied voltage at which the ionization integral becomes unity,

$$I = \int_0^{W_{epi}} A \exp \left[ - \left\{ b/E(x) \right\}^2 \right] dx = 1 \quad (10)$$

where  $E(x)$  is the electric field in V/cm,  $A = 3.5 \times 10^5$  /cm and  $b = 6.85 \times 10^5$  V/cm [7]. The electric field is obtained from the one dimensional Poisson's equation. The boundary conditions are imposed. The field is set to zero at  $x = W_{epi}$ .

Fig.6 shows the semiconductor layer structure for the hyperabrupt junction varactor. The epilayer thickness is 0.61 micron. Since MBE machines typically require manual adjustment of the doping level, a 'staircase' approximation has been used in implementing the hyperabrupt profile. The  $n^+$  layer thickness is 1.4 micron with a doping concentration of  $5 \times 10^{18} \text{ cm}^{-3}$ .

Fig.7 depicts a schematic of a planar mesa diode with air bridge. The parasitic components of this structure are shown in Fig.8. In the figure,  $C_p$  is the parasitic pad-to-pad capacitance,  $C_f$  is the capacitance between the anode contact finger and the  $n/n^+$  GaAs,  $L_s$  is the air bridge inductance,  $R_s$

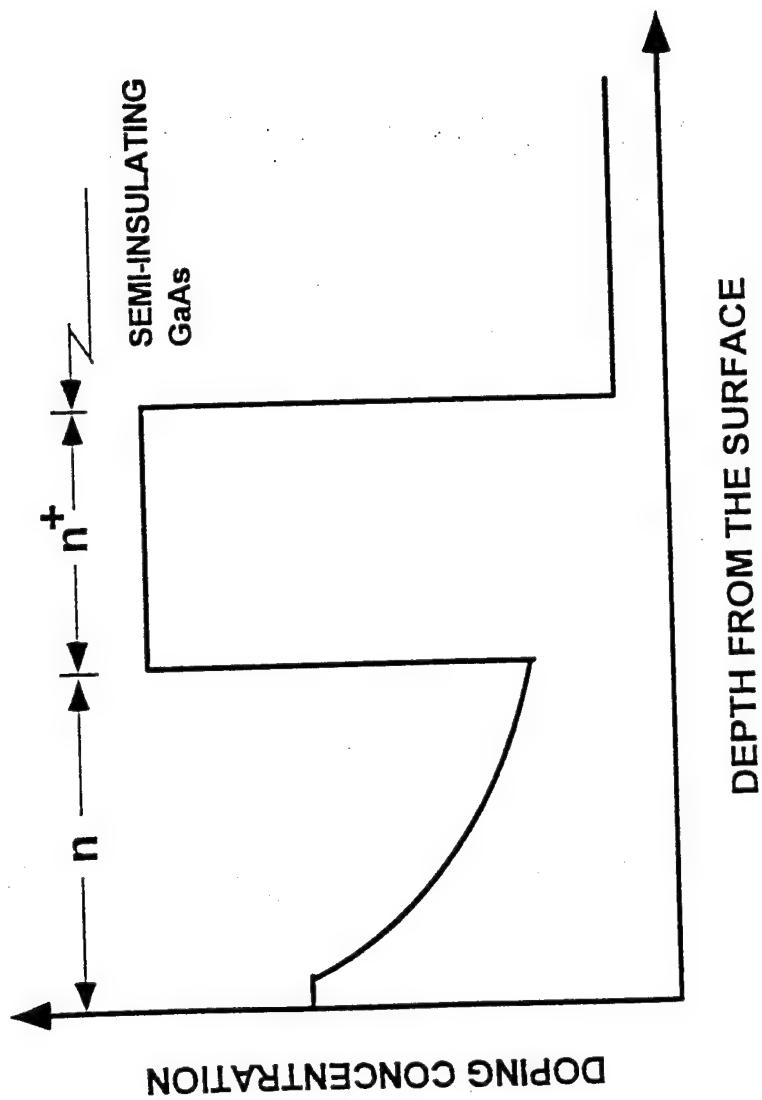


Figure 6 SEMICONDUCTOR LAYER STRUCTURE OF THE HYPERABRUPT VARACTOR

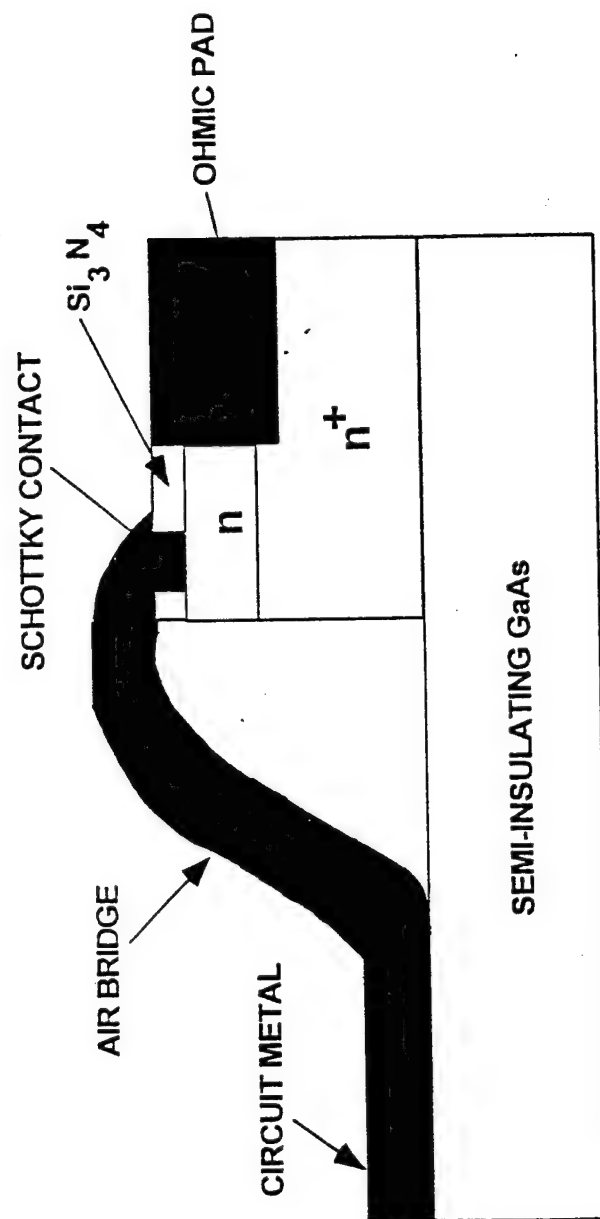


Figure 7 CROSS SECTION OF A PLANAR MESA DIODE WITH AN AIR BRIDGE

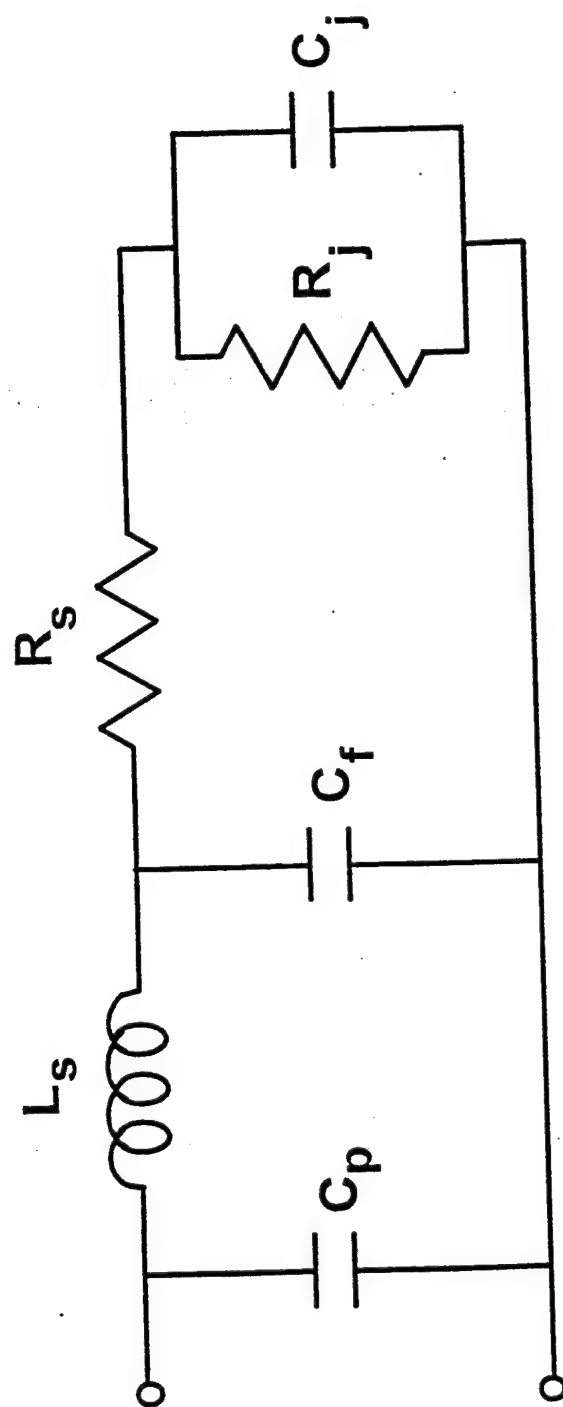


Figure 8 EQUIVALENT CIRCUIT WITH PARASITICS OF THE MESA DIODE



is the diode series resistance,  $R_j$  and  $C_j$  are the junction resistances and capacitances respectively.

### **2.0.2 DIODE GRID PHASE SHIFTER DESIGN**

The diode grid phase shifter is a square or rectangular mesh of metal strips on GaAs substrate. Fig.9 shows the periodic grid structure loaded with Schottky varactor diodes. The horizontal strips are used as bias lines. Changing reactance with bias controls the phase of the reflected wave. Design considerations include grid period, dielectric constant and angle of incidence. The design approach is based on transmission line theory and equivalent circuit model. This approach has been taken because it is relatively easy to incorporate both the diode model and supporting substrate into the analysis.

The transmission line model of the phase shifter grid periodically loaded with varactor diodes is shown in Fig.10. Each diode defines a unit cell of the grid. The grid needs to be optimized for incident signals at the design frequency by optimizing the dimensions and metal patterns of the unit cell and electrical properties of the grid substrate. Each diode in the array is presented with an embedding impedance which is a function of the grid structure repeated throughout each unit cell.

At the RF frequencies, quasi-optical reflection type diode grid phase shifter can be modelled as a two port network. The port 1 is the front of the grid itself, and the second port is the location in the grid unit cell where the diode is mounted. Obtaining the scattering parameters of an arbitrary quasi-optical grid phase shifter is a challenging problem. To date, solutions for *arbitrary shaped* unit cell metal patterns are still not available. However, significant progress has been made for specific metal patterns such as strips for grids assumed to be infinite in extent. Solutions make use of grid symmetry to reduce the problem of analyzing the entire grid to the simpler analysis of an equivalent waveguide unit cell. The equivalent waveguide then can be solved using techniques developed for the analysis of structures placed inside waveguides, or by the use of numerical three-dimensional finite element electromagnetic solvers. Solutions of this type, because they assume grids of infinite extent, completely ignore grid edge effects. Nevertheless, they have been found to provide reasonably good accuracy.

Let us assume an infinite grid with a uniform plane wave normally incident upon the grid surface. Symmetry then allows us to replace the

walls of the unit cell in the grid with electric and magnetic walls to form an equivalent waveguide unit cell. For the vertical electric field polarization, this waveguide has magnetic walls on the sides and electric walls on the top and bottom. The walls extend in the +z and -z directions, with the diodes in the  $z = 0$  plane. In effect this reduces the problem of analyzing the grid to that of analyzing an equivalent waveguide with electric and magnetic walls. The propagating mode is TEM, and the evanescent modes couple to the currents in the unit cell metal pattern.

It is desirable to keep the grid unit cell as small as possible to avoid the generation of undesirable substrate modes. If  $\lambda_d$  is the wavelength in the dielectric, then for unit cells larger than  $\lambda_d$ , substrate modes will begin to propagate. It should be reasonable to build grids as large as  $0.8 \lambda_d$ . For 94 GHz, this places the upper bound for the unit cell as  $710 \mu\text{m}$ .

Hewlett Packard's *High Frequency Structure Simulator* (HFSS) has been used to extract the embedding impedance of the complex geometry of the unit cell. To start with, a unit cell size of  $400 \mu\text{m} \times 400 \mu\text{m}$  with a vertical strip width of  $20 \mu\text{m}$  is used to design the grid for 94 GHz. Diode metal dimensions are included in the gap at the center of the strip. Fig.11 and 12 show the schematic of an unit cell and its simple equivalent circuit. Layouts of the HFSS waveguide cells used to simulate the grid design is shown in Fig.13. The de-embedded S-parameters are normalized to  $377 \Omega$ , the free space impedance. Computed S-parameters of the structure have been used to model the equivalent inductance and capacitance of the unit cell.

A simple transmission line model of the reflection grid phase shifter is shown in Fig.14. Free space is represented as a transmission line with a characteristic impedance of  $377 \Omega$ . The GaAs substrate appears as a section of the line with an impedance of  $105 \Omega$ . The substrate is backed by a metal short which serves as a reflector. In our first design we have not used any matching dielectric substrate on the front of the wafer. This will introduce impedance mismatch at the air/GaAs diode interface.

The above structure has been simulated using Touchstone to evaluate the phase range. The simulation is carried out for different junction capacitance values which varies with the DC bias voltage. The phase of the reflected wave and the reflection loss is calculated. Fig.15 shows the  $C_{\text{max}}/C_{\text{min}}$  versus phase shift plot calculated for  $C_{\text{max}} = 30 \text{ fF}$ . A maximum reflection loss of about -3 dB is calculated. Fig.16 shows the bias voltage versus phase shift plot for the same device.

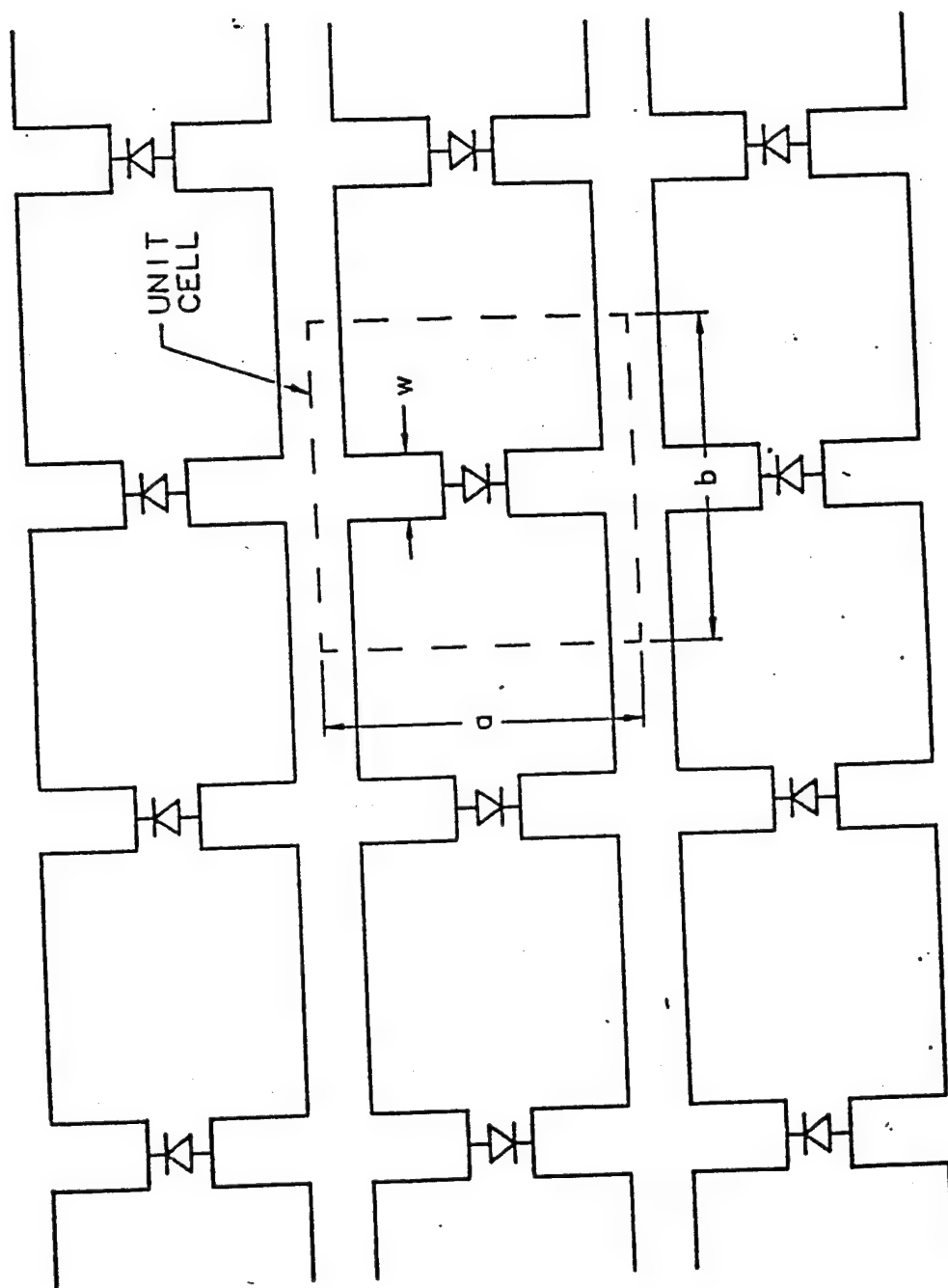


Figure 9 PERIODIC GRID STRUCTURE LOADED WITH SCHOTTKY  
VARACTOR DIODES

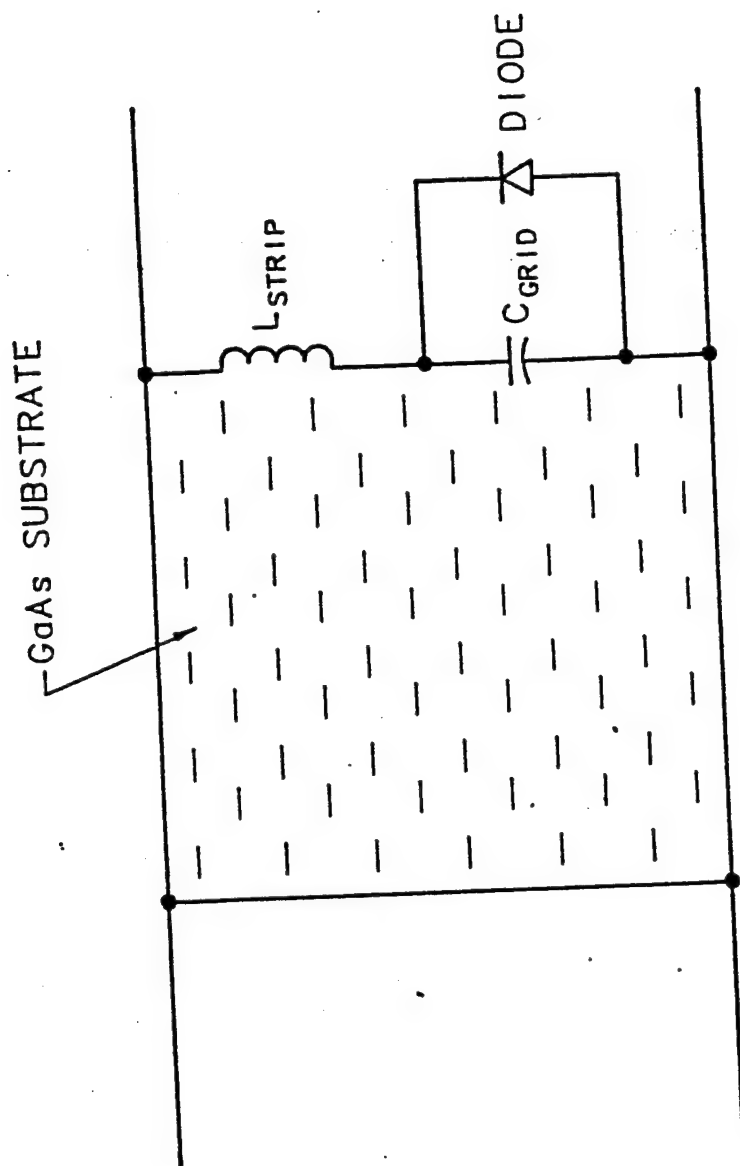


Figure 10 TRANSMISSION LINE MODEL OF THE ACTIVE GRID

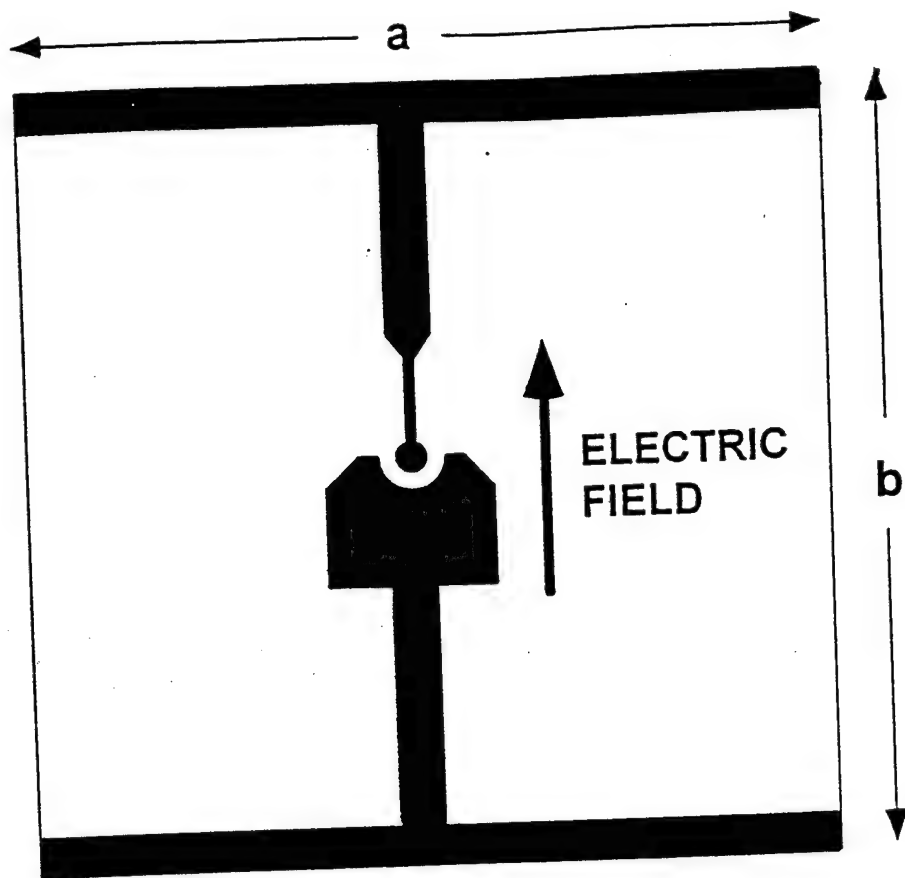


Figure 11 SCHEMATIC OF AN UNIT CELL

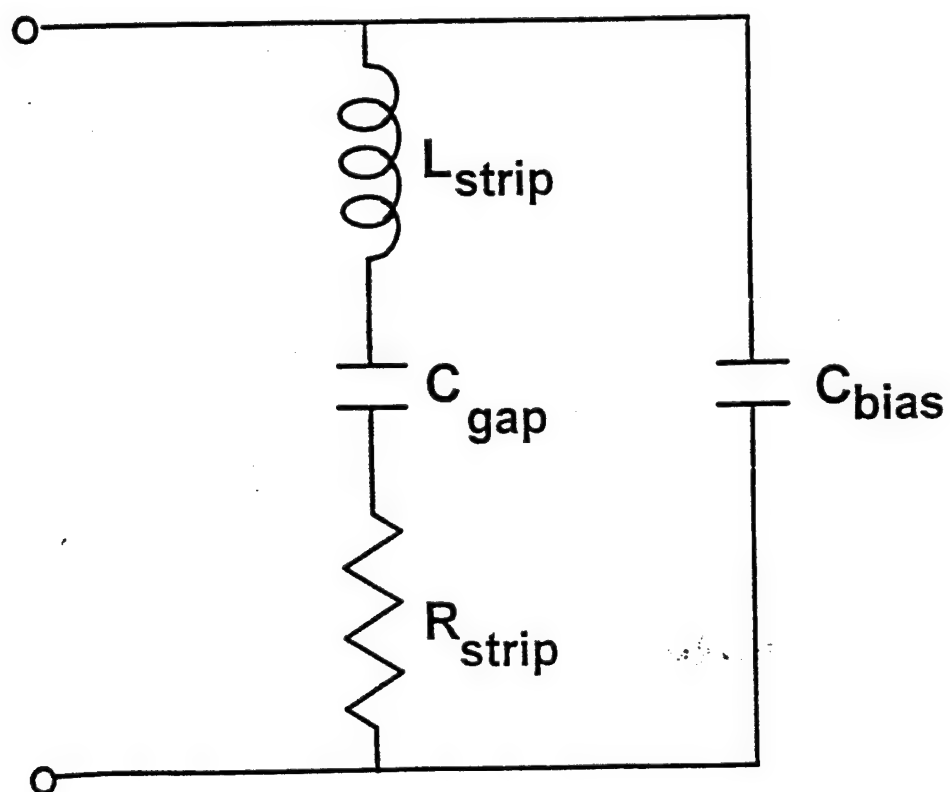


Figure 12 EQUIVALENT CIRCUIT OF A PASSIVE UNIT CELL

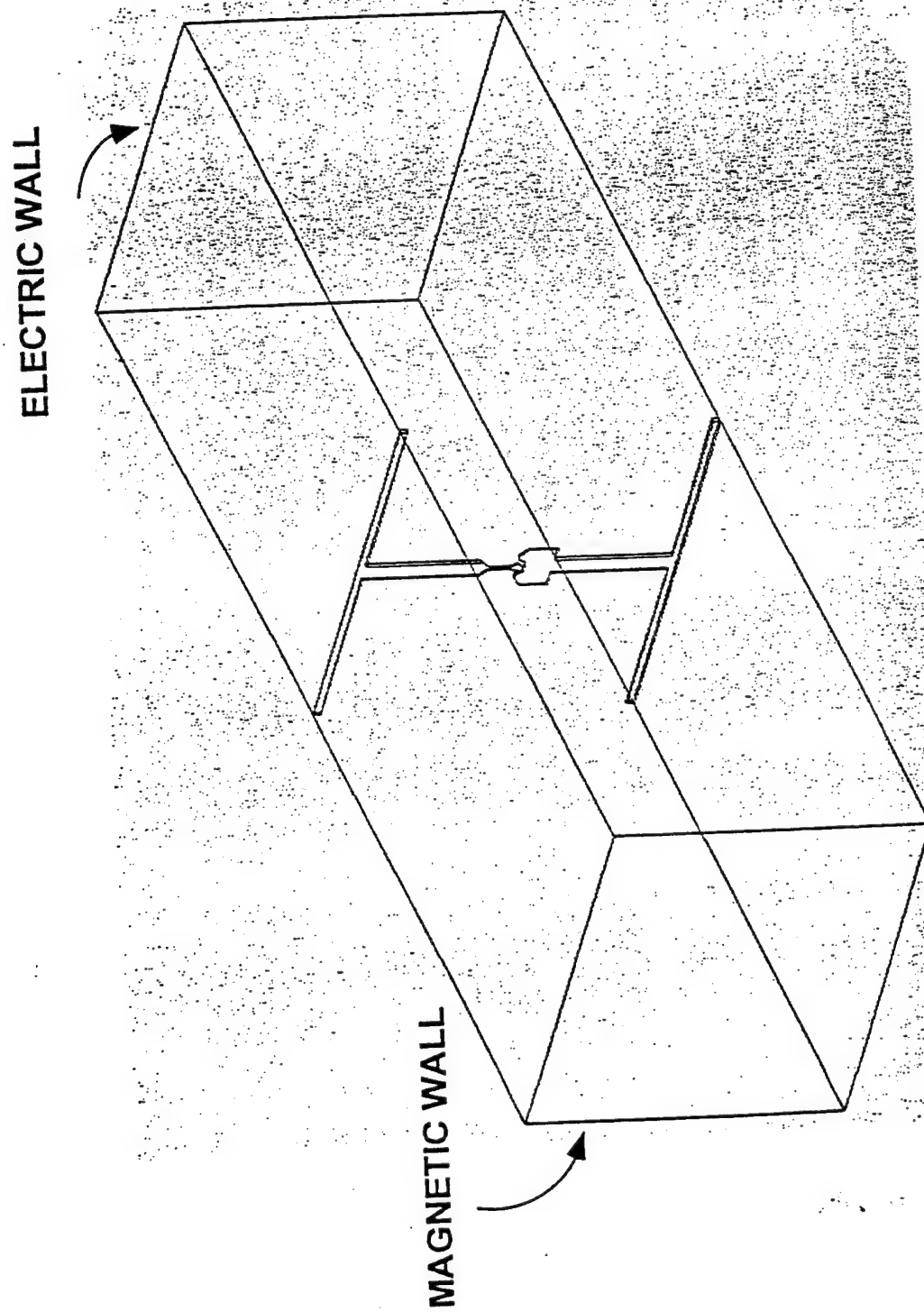


Figure 13 LAYOUT OF THE HFSS WAVEGUIDE CELLS

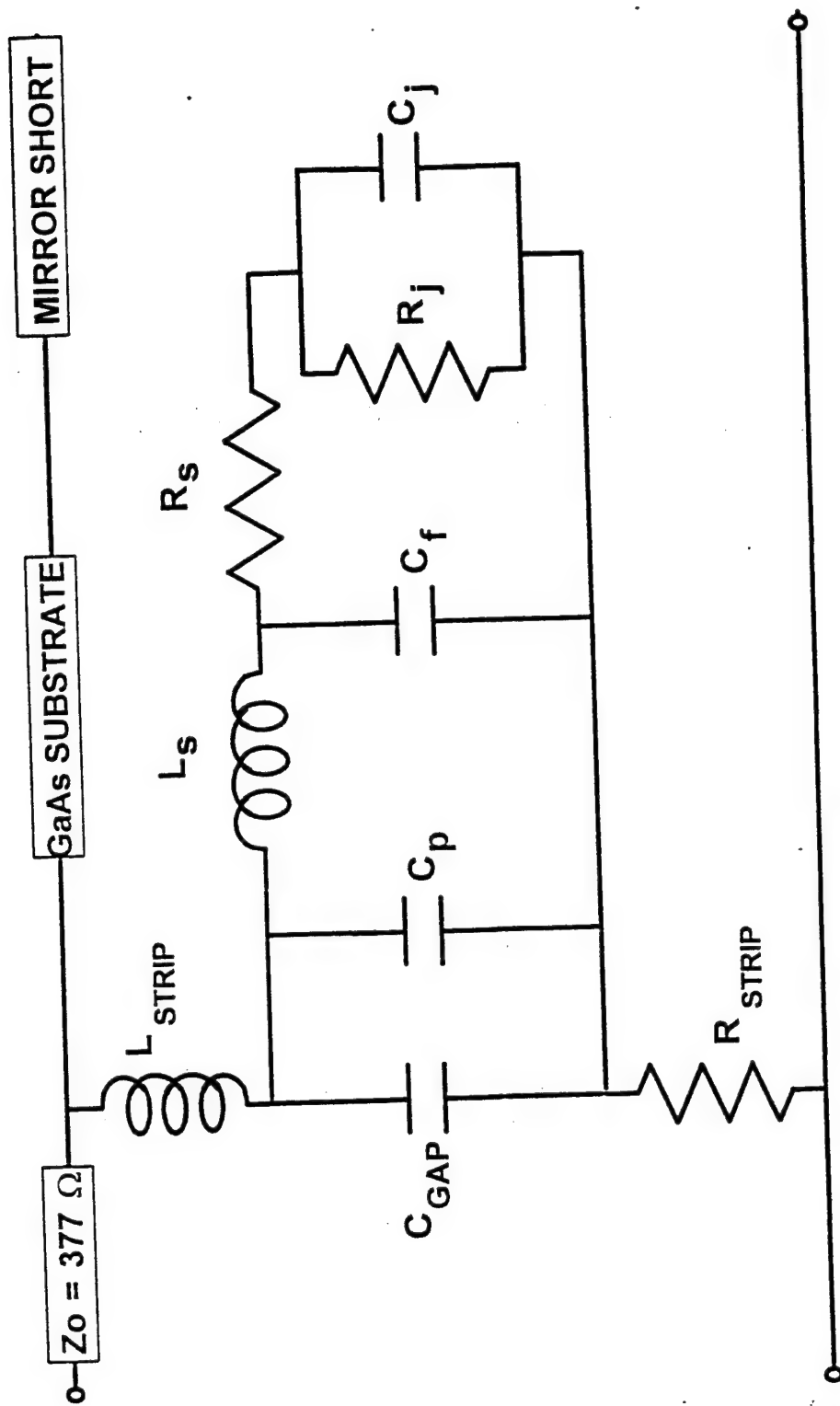


Figure 14 TRANSMISSION LINE EQUIVALENT CIRCUIT OF THE REFLECTION GRID PHASE SHIFTER

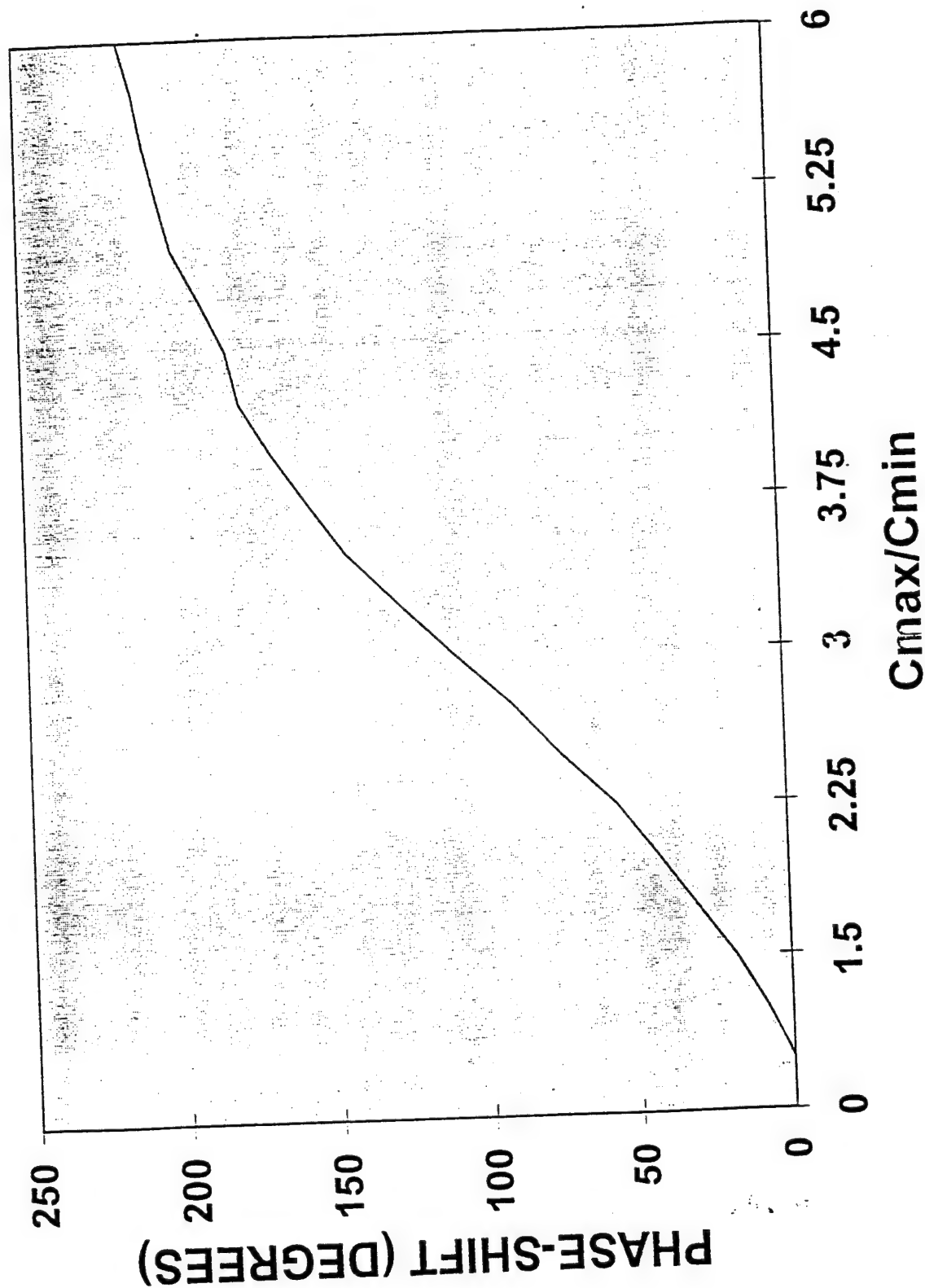


Figure 15 CALCULATED  $C_{max}/C_{min}$  VERSUS PHASE SHIFT PLOT FOR  
 $C_{max} = 30$  fF



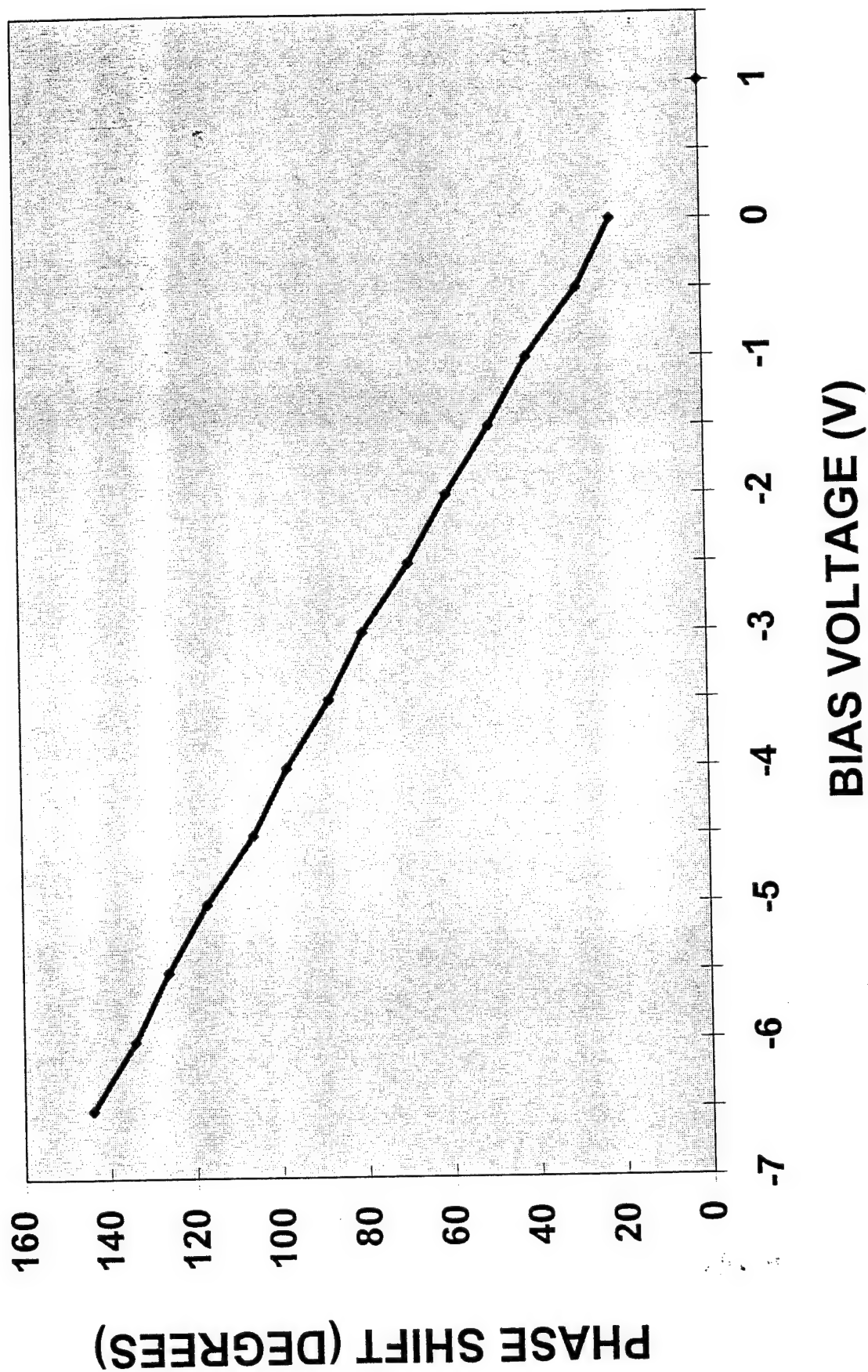


Figure 16 COMPUTED BIAS VOLTAGE VERSUS PHASE SHIFT PLOT  
FOR A DEVICE WITH  $C_{\max} = 30$  fF

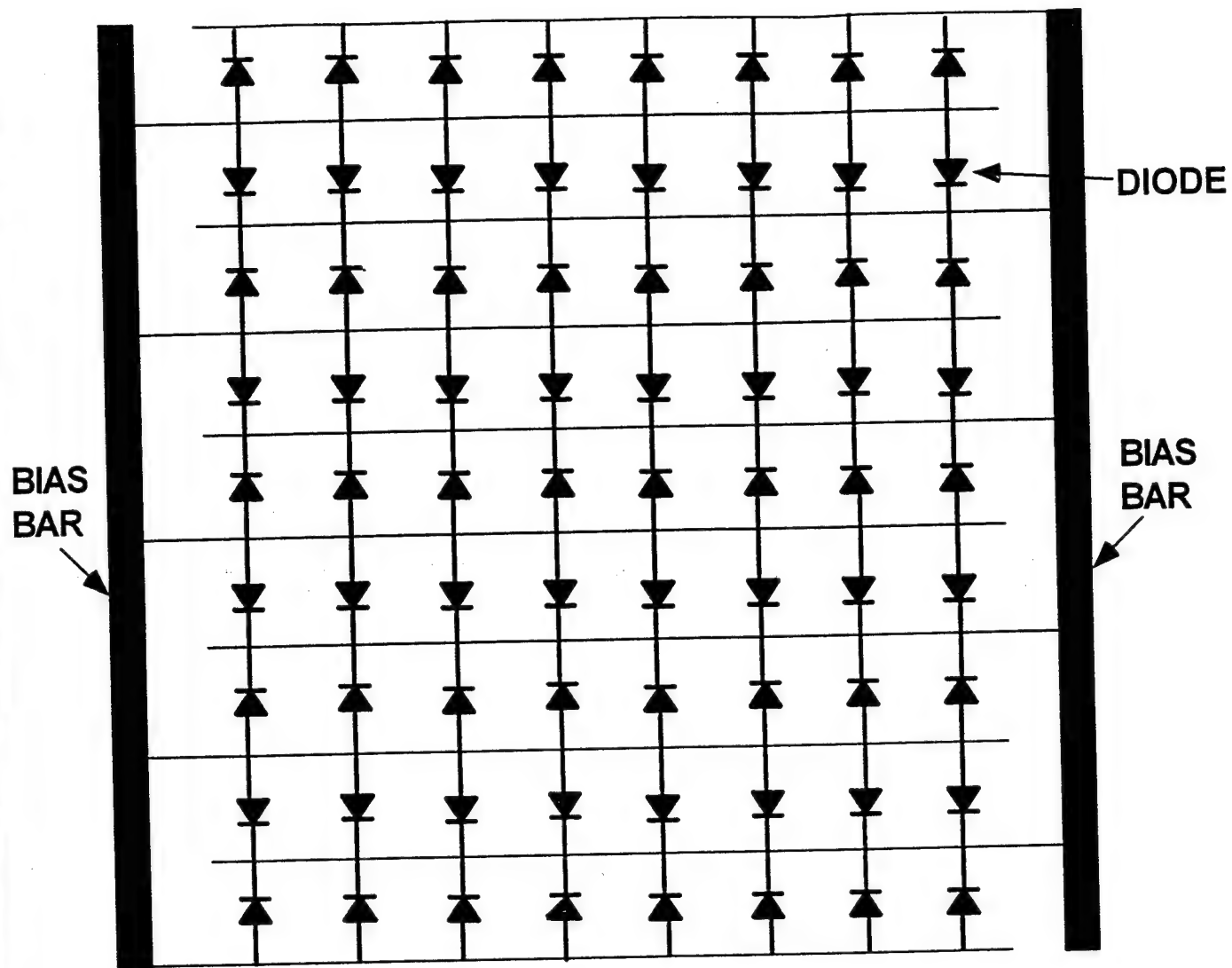


Figure 17 SCHEMATIC OF THE DIE SPA

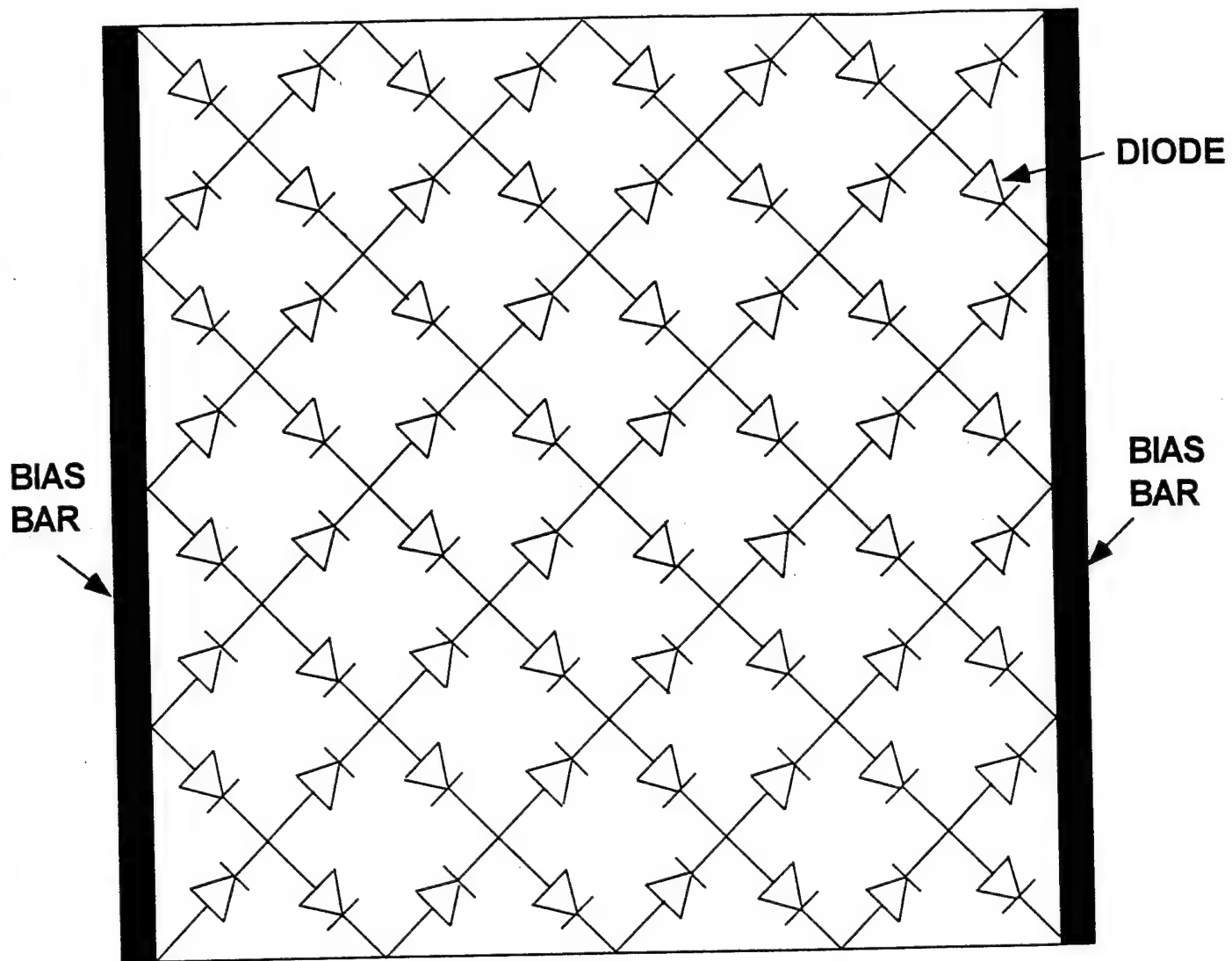


Figure 18 SCHEMATIC OF THE DIE DPA

We have proposed two different monolithic diode grid die designs. Fig.17 shows the schematic of the dies with diodes in only one direction (SPA). Fig.18 shows the concept of the monolithic dies with diodes in two perpendicular directions (DPA).

### **2.0.3 MONOLITHIC DIODE ARRAY FABRICATION AND DC RESULTS**

The fabrication of the monolithic varactor diode phase shifting arrays have been carried out in the Semiconductor Device Laboratory of Millitech. To begin the process, ohmic patterns are defined followed by Schottky metallization contacts. Mesas are then etched and subsequently circuit metal is defined. The wafer is then passivated by a dielectric. Dielectric windows are then opened to span plating contact metal.

Fig.19(a) and (b) show the photographs of the processed SPA and DPA dies respectively. Fig.20 shows the photograph of the device portion of the fabricated monolithic array.

Fig.21 shows the measured CV characteristic of a varactor diode with 5.4  $\mu\text{m}$  diameter. The ratio of the capacitance at zero bias to the capacitance at breakdown is about 4.9. The typical measured breakdown voltage is about -12V.

### **3.0 DRIVE CIRCUIT**

The circuit which will bias the full 115 mm diameter array of diodes was a task in the statement of work, however we supported the design with Millitech IR&D because of limited Phase 1 funds. Without such a circuit all of the diodes would be dc biased simultaneously with the result that there would be no phase gradient across the array. The circuit can arbitrarily bias each individual die and is controlled by a computer, which will scan the beam in a 4 x 4 point raster pattern. The 6 layers of this circuit are on both sides of 3 pieces of fiberglass. The first iteration of the photomasks for each layer are shown in Figure 22.

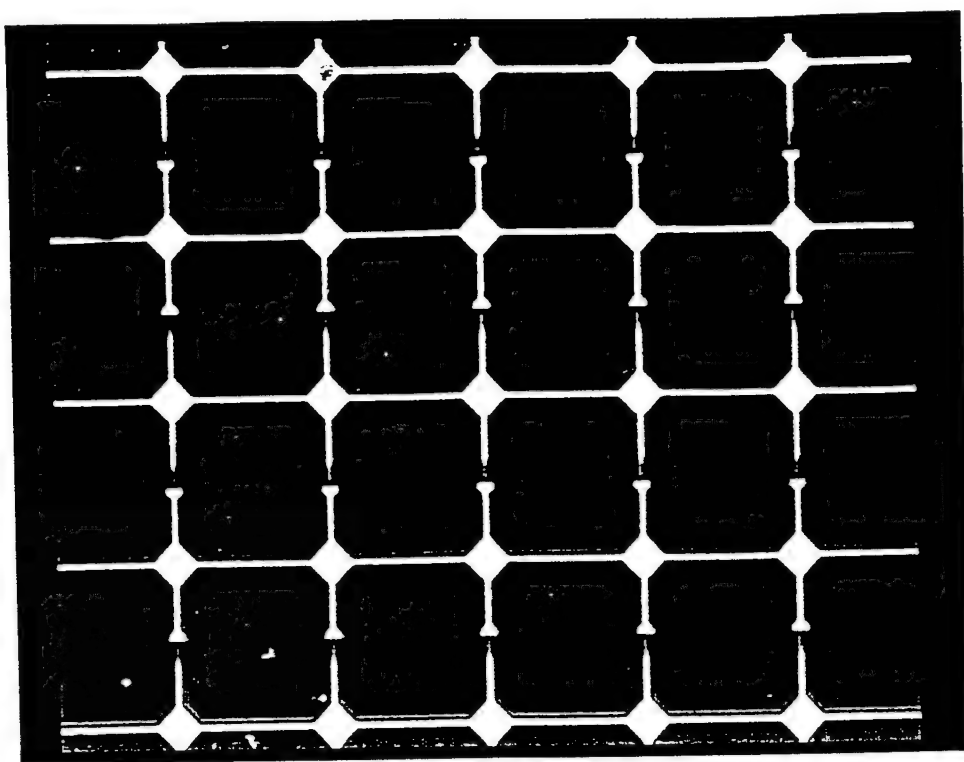


Figure 19(a) PHOTOGRAPH OF THE PROCESSED MONOLITHIC SPA DIE

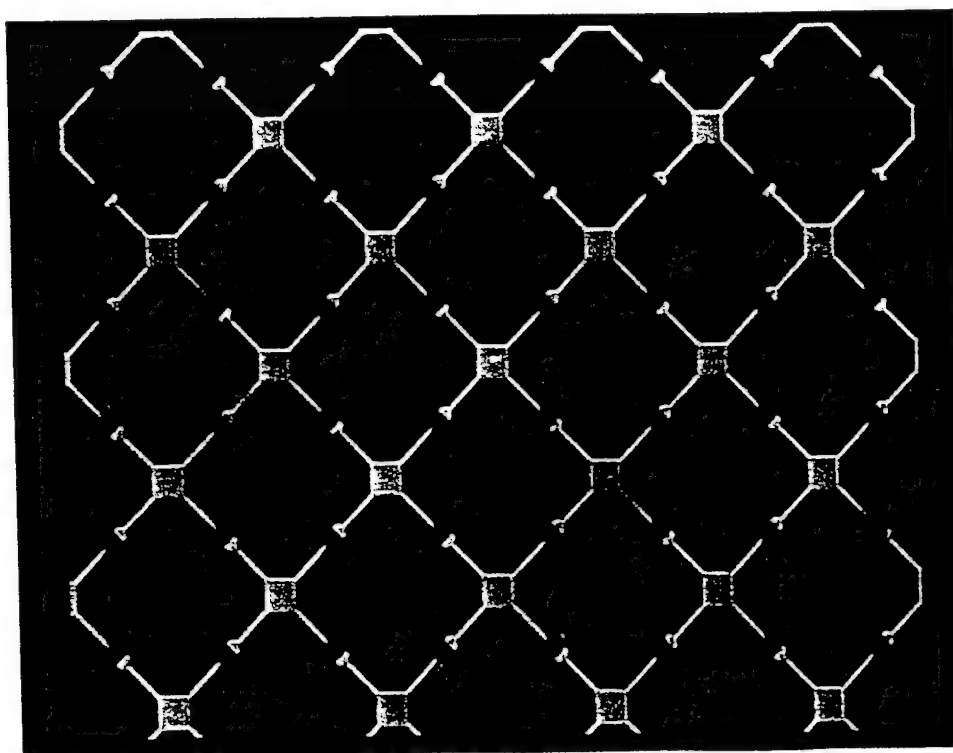
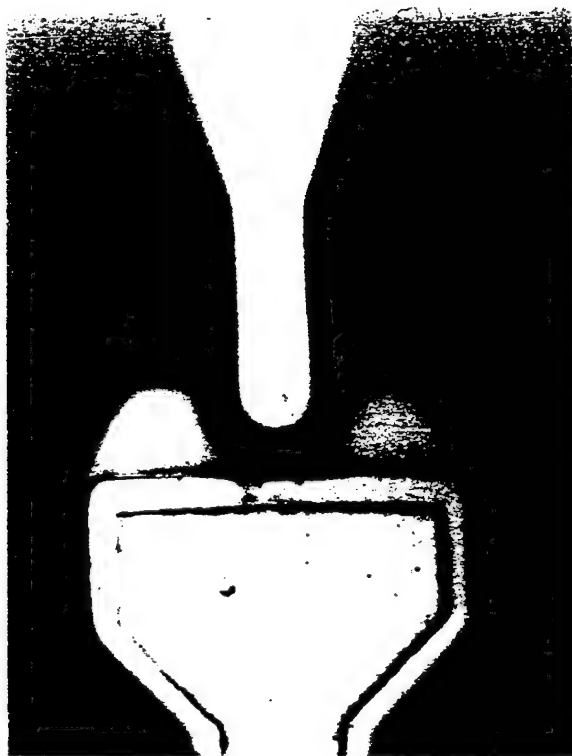


Figure 19(b) PHOTOGRAPH OF THE PROCESSED MONOLITHIC DPA DIE



**Figure 20** CLOSE-UP OF THE DEVICE PORTION OF THE MONOLITHIC ARRAY

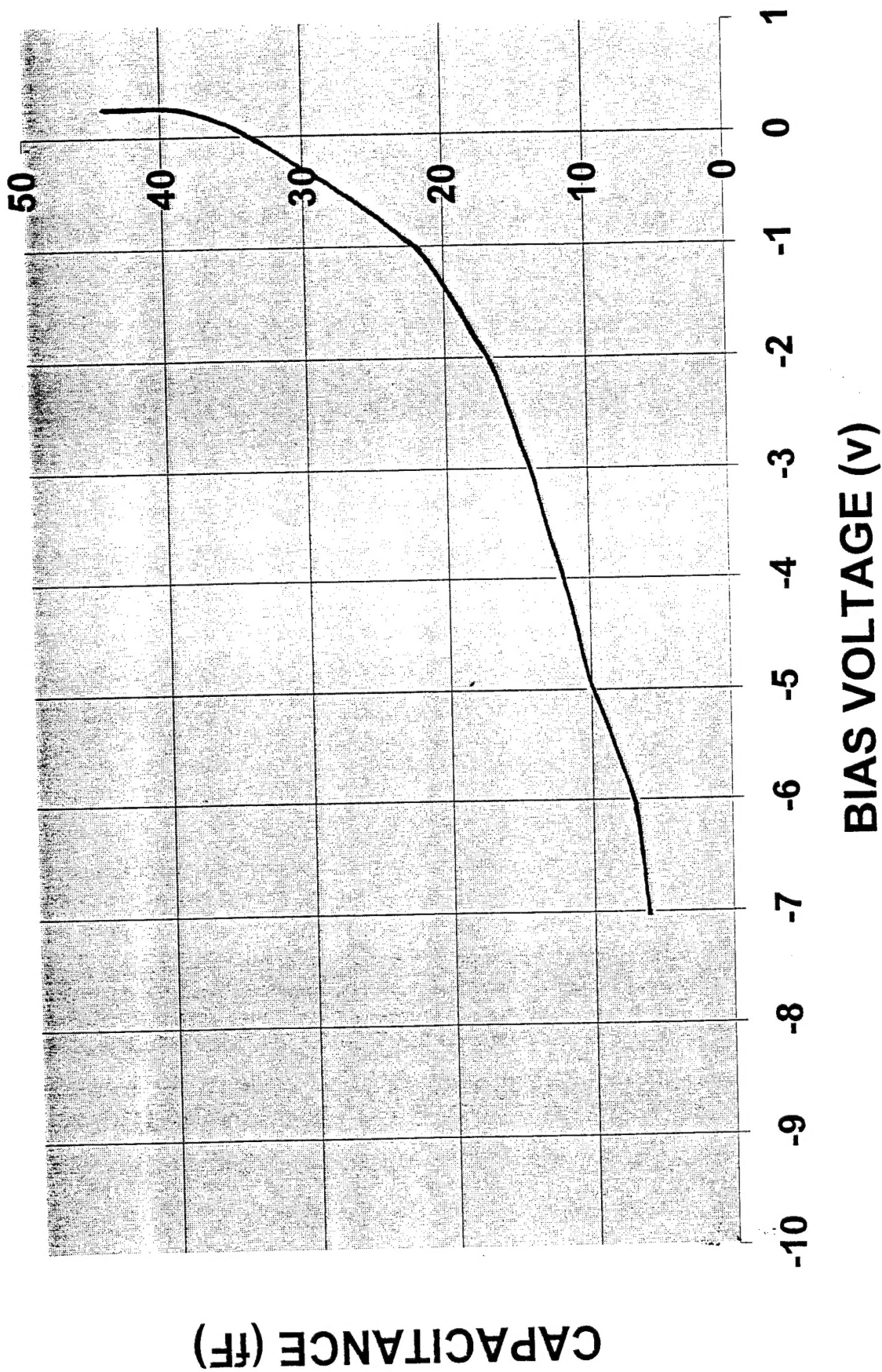


Figure 21 MEASURED C-V CHARACTERISTIC OF AN ARRAY VARACTOR  
DEVICE (ANODE DIAMETER = 5.4  $\mu\text{m}$ )

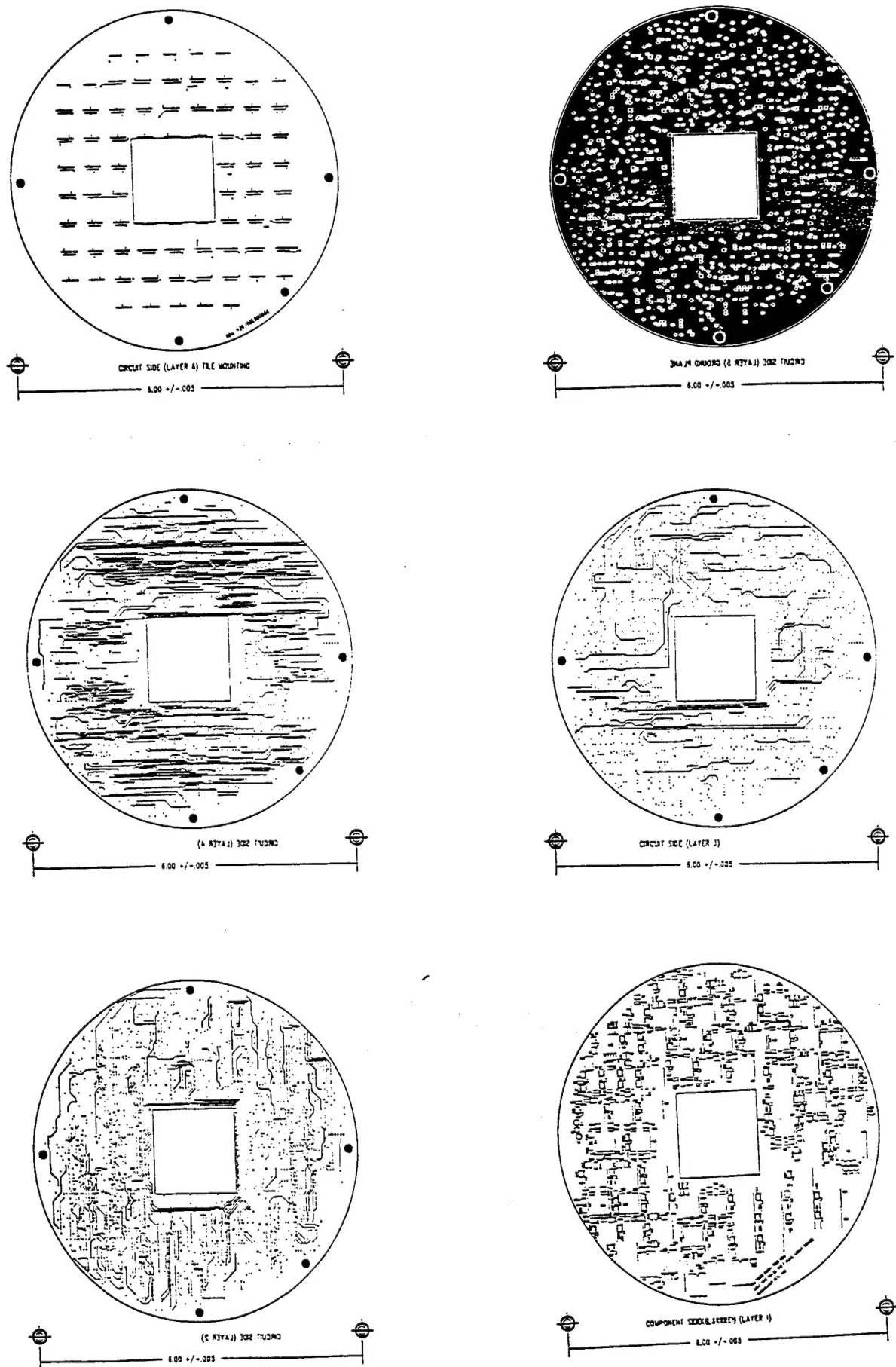


Figure 22 FIRST ITERATION OF THE PHOTOMASKS FOR EACH LAYER OF THE DRIVE CIRCUIT



#### **4.0 RF TEST SET UP STATUS**

The phase shift test set-up described in the quarterly progress report is expected to be complete by mid-May. The only outstanding circuit components are the two subharmonic mixers, and the quasioptical components and fixtures will be completed by May 10. We are getting quotations for a near field range to measure the complete phase shifting array beam patterns during Phase 2.

#### **5.0 PHASE 2 PLANS**

Phase 2 will contain the tasks listed below.

1. All RF measurements
2. Beam steering pattern prediction
3. Modifications to the die based on DC and RF test results. We expect three iterations including the design described in this report.
4. Build and test a small array of dies, 2x2 or 3x3. This will indicate the ease of manufacturing and assembling. An array larger than 12.7x12.7 mm<sup>2</sup> die will be easier to test on the quasioptical set-up and give a larger aperture array for better RF results.
5. Build the 6-layer drive circuit for the 115 mm diameter beam steering array.
6. Build the 115 mm beam steering array.
7. Test the beam steering array on the near field range.

Some of these tasks will exceed the \$375,000 limit and will be included in an addendum of the Phase 2 proposal.

#### **6.0 SUMMARY AND CONCLUSIONS**

The results of the phase 1 effort include Schottky varactor diode design, quasioptical mesh circuit design, development of 12.7 mm dies incorporating these designs and DC testing of varactor diodes. The measured CV and IV characteristics of the diodes are close to the design values. We have also designed a 115 mm diameter monolithic beam steering array and drive circuit, which will be manufactured and tested during Phase 2. The quasioptical phase shifting set-up is almost complete and we expect to begin RF tests on the 12.7 mm dies by mid-May. During phase 2, we will upgrade our RF test set-up to include a small near field

range to measure the beam steering capability of the 115 mm monolithic array.

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